DATA SHEET

# M3202A PXIe Arbitrary Waveform Generator with Optional Real-Time Sequencing and FPGA Programming

1 GSa/s, 14 Bits, 4 Channels


## Generate High-Precision, Complex, Real-World Signals

The M3202A high-performance, high-bandwidth arbitrary waveform generator combines an advanced waveform generation system with embedded function generators and modulators (frequency/phase/amplitude) for broadband and IF signal generation. Performance meets simplicity thanks to easy-to-use programming libraries, real-time sequencing technology (Hard Virtual Instrumentation or HVI technology), and graphical FPGA programming technology.

## Features

- 1 GS/s, 14 bits, 4 ch, 400 MHz BW (800 MHz IQ)
- Embedded advanced arbitrary waveform generators (AWGs)
  - Advanced triggering and marking (up to 8 reconfigurable I/Os)
  - Waveform queue system with cycles, delays and prescalers
- Embedded high-precision function generators (FGs)
  - Sinusoidal, triangular, square, DC, and more
  - 45-bit frequency resolution (up to ~ 5.68 µHz)
  - 24-bit phase resolution (up to ~ 21.5 µdeg)
- Embedded ultra-flexible amplitude and angle modulators
- High-quality output signal with low phase noise
  - SFDR: ~ 54 dBc @160 MHz
  - Average noise density: down to ~ –145 dBm/Hz
- Optional features
  - Simultaneous amplitude and angle modulations
- Up to 2 GB of onboard RAM (~ 1 Gsamples)
- Mechanical/interface
  - 1 slot 3U (PXIe)
  - PCIe Gen2
  - Independent direct memory access (DMA) channels for fast and efficient data transfer

**Applications**

Quantum computing, 5G research

Manufacturing in wireless devices, automated test equipment (ATE)

MIMO, beam forming and other multi-channel coherent signal generation

General purpose, RF/arbitrary waveform generation

R&D/scientific research equipment, aerospace and defense (A/D)

KEYSIGHT TECHNOLOGIES

# Programming Technology and Software Tools

## Software programming

- Easy-to-use native programming libraries for most common languages: C, C++, Visual Studio, LabVIEW, MATLAB, and Python

## Hardware programming (optional)

- Real-time sequencing (Hard Virtual Instrumentation or HVI technology)
  - Ultra-fast, fully-parallelized, hard real-time execution
  - Ultra-fast, time-deterministic decision-making
  - Off-the-shelf inter-module synchronization and data exchange
- FPGA programming
  - FPGA design environment and BSP support
  - Supports VHDL, Verilog and Xilinx projects, and Xilinx IP Catalog
  - Ultra-fast, one-click compiling and on-the-fly programming

## SD1 2.x and SD1 3.x differences

Keysight SD1 2.x software has been upgraded to 3.x. The key differences are listed in the table below. For more detail on SD1 3.x software, refer to the Start Up Guide M3xxx-90002.

[WARNING] The 3.X version of software does not support programs using the M3601A or the M3602A applications. You will have to transition to KS2201A and KF9000A respectively.

| SD1 software features | Legacy (SD1 2.1.x) | New (SD1 3.x) |
|---|---|---|
| **Software** | | |
| Design Environment | M3601A HVI design environment (ProcessFlow) | KS2201A PathWave Test Sync Executive (HVI2 technology) |
| | M3602A FPGA design environment (FPGAFlow) | KF9000A PathWave FPGA Programming |
| | | Environment (commonly known as PathWave FPGA) |
| HVI Technology | Graphical M3601A for HV1 | KS2201A PathWave Test Sync Executive (HVI2 Core API through a separate HVI installer) |
| | HVI-C API (through SD1 installer) | |
| FPGA Programming | Graphical M3602A | PathWave FPGA (BSP installer for each supported module is required) |
| | PathWave FPGA (BSP for SD1 2.1.x only) | |
| Soft Front Panel (SFP) | Available | Available |
| Programming Interface | Python, C++, C#, LabVIEW, MATLAB | Python, C, C++, C# |
| Supported Operating System | Windows 10 | Windows 10 |

| SD1 software features | Legacy (SD1 2.1.x) | New (SD1 3.x) |
|---|---|---|
| **Hardware modules** | | |
| M3202A (AWG 1G) | FW version < 4.0 (CH4) (CLF) (K16, K32, K41) | FW version > =4.0 (CH4) (CLF) (K16, K32, K41) |
| | BSP available (K32, K41) | BSP available (K32, K41) |
| M3201A (AWG 500) | FW version < 4.0 (CH4) (CLF) (K16, K32, K41) | FW version > =4.0 (CH4) (CLF) (K16, K32, K41) |
| | BSP available (K32, K41) | BSP available (K32, K41) |
| M3102A (DIG 500) | FW version < 2.0 (CH4) (CLF) (K16, K32, K41) | FW version > =2.0 (CH4) (CLF) (K16, K32, K41) |
| | BSP available (K32, K41) | BSP available (K32, K41) |
| M3100A (DIG 100) | FW version < 2.0 (CH4 or CH8) (CLF) (K16, K32, K41) | FW version > =2.0 (CH4) (CLF) (K32, K41) |
| | BSP available (K32, K41) | BSP not available |
| M3302A (COMBO 500 500) | FW version < 4.0 (CH2 AWG - CH2 DIG) (CLF) (K32, K41) | FW version > =4.0 (CH2 AWG - CH2 DIG) (CLF) (K41) |
| | BSP available (K32, K41) | BSP not available |
| M3300A (COMBO 500 100) | FW version < 4.0 (CH2 AWG - CH4 DIG or CH4 AWG - CH8 DIG) (CLF) (K32, K41) | FW version > =4.0 (CH2 AWG - CH4 DIG) (CLF) (K41) |
| | BSP available (K32) | BSP not available |
| **No programming** | | |
| Easily configurable SD1 SFP (software front panel) interface for each connected module | | |

## PXIe Arbitrary Waveform Generators, Digitizers and Combination Modules

| Product | Type | Outputs (AWGs) | | | | Inputs (Digitizers) | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | Speed (MSa/s) | Bits | Ch | BW (MHz) | Speed (MSa/s) | Bits | Ch | BW (MHz) |
| M3202A | AWG | 1000 | 14 | 4 | DC-400 | | | | |
| M3201A | AWG | 500 | 16 | 4 | DC-200 | | | | |
| M3102A | Digitizer | | | | | 500 | 14 | 4 | DC-200 |
| M3100A | Digitizer | | | | | 100 | 14 | 4/8 | DC-100 |
| M3302A | Combo | 500 | 16 | 2 | DC-200 | 500 | 14 | 2 | DC-200 |
| M3300A | Combo | 500 | 16 | 2/4 | DC-200 | 100 | 14 | 4/8 | DC-100 |

Note: For SD1 3.x M3100A and M3300A only come in a 4 channel Digitizer version. And M3300A in the 2 channel AWG version.

## Functional Block Diagram

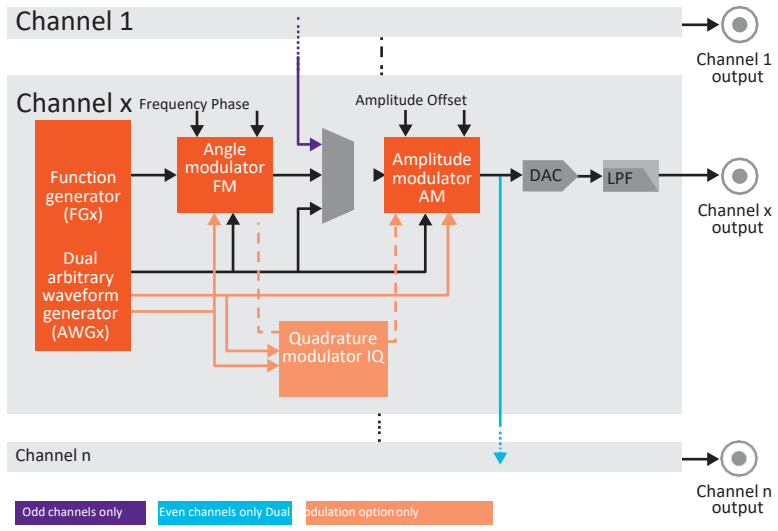


Figure 1. M3201A output functional block diagram, all channels have identical output structure

## Ordering Information [1]

| Product | Description |
|---|---|
| M3202A | PXI arbitrary waveform generator: 1 GSa/s, 14 Bits |
| **Options** | **Description** |
| M3202A-CH4 | Four channels |
| M3202A-CLF | Fixed sampling clock, low jitter |
| M3202A-DM1 | Dual modulation capability (amplitude and angle simultaneously) |
| M3202A-M01 / -M12 / -M20 | Memory [2] 16 MB, 8 MSamples / 128 MB, 60 MSamples / 2 GB, 1 GSamples |
| **Options** | **License option** |
| M3601A | HVI design environment |
| M3602A | FPGA design environment |
| KS2201A | PathWave Test Sync Executive |
| KF9000A | Pathwave FPGA |

1. All options must be selected at time of purchase and are not upgradable.
2. These options represent the standard configuration.

# Technical Specifications and Characteristics

## General characteristics

| Parameter | M3202A-CH4 | | | Units | Comments |
|---|---|---|---|---|---|
| | Min | Typ | Max | | |
| **Inputs and outputs** | | | | | |
| Channels (single-ended mode) | | 4 | | Out | |
| Channels (differential mode) | | 2 | | Out | Differential uses 2 channels |
| Reference clock [1] | | 1 | | Out | |
| Reference clock [2] | | 1 | | In | |
| Triggers/markers [1, 3] | | 1 | | In/out | Reconfigurable |
| Triggers/markers [2, 3] | | 8 | | In/out | Reconfigurable |
| **Output channels overview** | | | | | |
| Sampling rate | | 1000 | | MSa/s | |
| Voltage resolution | | 14 | | Bits | |
| Output frequency | DC | | 400 | MHz | |
| Real-time BW | | 400 | | MHz | |
| Output voltage | –1.5 | | 1.5 | Volts | |
| **Built-in functionalities** | | | | | |
| Function generators | | 4 | | | 1 per channel |
| Dual AWGs | | 4 | | | 1 per channel |
| IQ modulators | | 4 | | | 1 per channel |
| Frequency modulators | | 4 | | | 1 per channel |
| Phase modulators | | 4 | | | 1 per channel |
| Amplitude modulators | | 4 | | | 1 per channel |
| DC offset modulators | | 4 | | | 1 per channel |
| **Onboard memory** | | | | | |
| RAM memory | 16 | | 2048 | MBytes | |

1. At front panel.
2. At backplane.
3. Markers available from firmware version v3.0 or later.

## I/O specifications

| Parameter | M3202A-CH4 | | | Units | Comments |
|---|---|---|---|---|---|
| | Min | Typ | Max | | |
| **Output channels** | | | | | |
| Sampling rate | 1.0 | | | GSa/s | |
| Output frequency | DC | | 400 | MHz | Limited by a reconstruction filter |
| Output voltage | –1.5 | | 1.5 | $V_p$ | On a 50 Ω load |
| Source impedance | 50 | | | Ω | |
| **Reference clock output** | | | | | |
| Frequency | 10 or 100 | | | MHz | Generated from the internal clock, user selectable |
| Voltage | 800 | | | $mV_{pp}$ | On a 50 Ω load |
| Power | 2 | | | dBm | On a 50 Ω load |
| Source impedance | 50 | | | Ω | AC coupled |
| **External I/O trigger/marker** | | | | | |
| $V_{IH}$ | 2 | | 5 | V | |
| $V_{IL}$ | 0 | | 0.8 | V | |
| $V_{OH}$ | 2.4 | | 3.3 | V | On a high Z load |
| $V_{OL}$ | 0 | | 0.5 | V | On a high Z load |
| Input impedance | 10 | | | KΩ | |
| Source impedance | TTL | | | – | |
| Speed | 100 | | | MHz | |

## Function generators (FGs) specifications

| Parameter | M3202A-CH4 | | | Units | Comments |
|---|---|---|---|---|---|
| | Min | Typ | Max | | |
| **General specifications** | | | | | |
| Function generators | | 4 | | – | 1 per channel |
| Waveform types | | 4 | | – | Sinusoidal, triangular, square and DC |
| Frequency range | 0 | | 400 | MHz | |
| Frequency resolution | | 45 | | Bits | |
| Frequency resolution | | 11.4 | | µHz | |
| Phase range | 0 | | 360 | Deg | |
| Phase resolution | | 24 | | Bits | |
| Phase resolution | | 21.5 | | µdeg | |
| **Speed performance** | | | | | |
| Frequency change rate | | 100 | | MChanges/s | With HVI technology |
| Frequency modulation rate | | 1000 | | MSamples/s | With AWGs and angle modulators |
| Phase change rate | | 100 | | MChanges/s | With HVI technology |
| Phase modulation rate | | 1000 | | MSamples/s | With AWGs and angle modulators |

## Amplitude and offset specifications

| Parameter | M3202A-CH4 | | | Units | Comments |
|---|---|---|---|---|---|
| | Min | Typ | Max | | |
| **General specifications** | | | | | |
| Amplitude / offset range | –1.5 | | 1.5 | $V_p$ | Amplitude + offset values |
| Amplitude / offset resolution | | 14 | | Bits | |
| Amplitude / offset resolution | | 183.1 | | µV | |
| **Speed performance** | | | | | |
| Amplitude / offset change rate | | 1000 | | MChanges/s | With HVI technology |
| Amplitude / offset modulation rate | | 1000 | | MSamples/s | With AWGs and amplitude modulators |

## Arbitrary waveform generators (AWGs) specifications

| Parameter | M3202A-CH4 | | | Units | Comments |
|---|---|---|---|---|---|
| | Min | Typ | Max | | |
| **General specifications** | | | | | |
| Dual AWGs | | 4 | | | 1 dual AWG per output channel |
| Aggregated speed (16 bits) | | | 4 | GSa/s | For all onboard waveforms combined |
| Aggregated speed (32 bits) | | | 2 | GSa/s | For all onboard waveforms combined |
| Waveform multiple | | 5 | | Samples | Waveform length must be a multiple of this value |
| 16-bit waveform length | 65 | | 957 | MSamples | Maximum depends on onboard RAM |
| 32-bit waveform length | 65 | | 478 | MSamples | Maximum depends on onboard RAM |
| Waveform length efficiency | | 93.5 | | % | Efficiency = waveform size / waveform size in RAM |
| Trigger | | Select | | | External trigger (input connector, backplane triggers), SW/HVI trigger |
| **AWG specifications (16-bit single waveform)** | | | | | |
| Speed | | | 1 | GSa/s | Per AWG |
| Resolution | | 16 | | Bits | |
| AWG destination | | Select | | | Amplitude, offset, frequency or phase |
| **AWG specifications (16-bit dual waveform)** | | | | | |
| Speed (waveform A) | | | 1 | GSa/s | Per AWG |
| Speed (waveform B) | | | 1 | GSa/s | Per AWG |
| Resolution (waveform A) | | 16 | | Bits | |
| Resolution (waveform B) | | 16 | | Bits | |
| AWG destination (waveform A) | | Select | | | Amplitude and offset or I and Q control outputs on channels |
| AWG destination (waveform B) | | Select | | | Frequency and phase or I and Q readouts on channels |
| **AWG specifications (32-bit single waveform)** | | | | | |
| Speed | | | 0.1 | GSa/s | Per AWG, minimum prescaler: 1 |
| Resolution | | 32 | | Bits | |
| AWG destination | | Select | | | Amplitude, offset, frequency or phase |

| Parameter | M3202A-CH4 | | | Units | Comments |
|---|---|---|---|---|---|
| | Min | Typ | Max | | |
| **AWG specifications (32-bit dual waveform)** | | | | | |
| Speed (waveform A) | | | 0.1 | GSa/s | Per AWG, minimum prescaler: 1 |
| Speed (waveform B) | | | 0.1 | GSa/s | Per AWG, minimum prescaler: 1 |
| Resolution (waveform A) | | 32 | | Bits | |
| Resolution (waveform B) | | 32 | | Bits | |
| AWG destination (waveform A) | | Select | | | Amplitude or offset |
| AWG destination (waveform B) | | Select | | | Frequency or phase |

## Angle modulators specifications

| Parameter | M3202A-CH4 | | | Units | Comments |
|---|---|---|---|---|---|
| | Min | Typ | Max | | |
| **General specifications** | | | | | |
| Frequency modulators | | 4 | | | 1 per output channel |
| Phase modulators | | 4 | | | 1 per output channel |
| Carrier signal source | | FGs | | | Refer to the FG specifications table in this document |
| Modulating signal source | | AWGs | | | Refer to the AWG specifications table in this document |
| **Frequency modulators (16-bit modulating waveform)** | | | | | |
| Deviation | –Dev. gain | | +Dev. gain | MHz | |
| Modulating signal resolution | | 16 | | Bits | AWG waveform |
| Modulating signal BW | 0 | | 500 | MHz | AWG Nyquist limit |
| Deviation gain | 0 | | 400 | MHz | |
| Deviation gain resolution | | 16 | | Bits | |
| **Frequency modulators (32-bit modulating waveform)** | | | | | |
| Deviation | –Dev. gain | | +Dev. gain | MHz | |
| Modulating signal resolution | | 32 | | Bits | AWG waveform |
| Modulating signal BW | 0 | | 100 | MHz | AWG Nyquist limit |
| Deviation gain | 0 | | 400 | MHz | |
| Deviation gain resolution | | 16 | | Bits | |
| **Phase modulators (16-bit modulating waveform)** | | | | | |
| Deviation | –Dev. gain | | +Dev. gain | Deg | |
| Modulating signal resolution | | 16 | | Bits | AWG waveform |
| Modulating signal BW | 0 | | 500 | MHz | AWG Nyquist limit |
| Deviation gain | 0 | | 180 | Deg | |
| Deviation gain resolution | | 16 | | Bits | ~ 5.5 mdeg |
| **Phase modulators (32-bit modulating waveform)** | | | | | |
| Deviation | –Dev. gain | | +Dev. gain | Deg | |
| Modulating signal resolution | | 16 | | Bits | AWG waveform is truncated |
| Modulating signal BW | 0 | | 100 | MHz | AWG Nyquist limit |
| Deviation gain | 0 | | 180 | Deg | |
| Deviation gain resolution | | 16 | | Bits | ~ 5.5 mdeg |

## Amplitude modulators specifications

| Parameter | M3202A-CH4 | | | Units | Comments |
|---|---|---|---|---|---|
| | Min | Typ | Max | | |
| **General specifications** | | | | | |
| Amplitude modulators | | 4 | | | 1 per output channel |
| Offset modulators | | 4 | | | 1 per output channel |
| Carrier signal source | | FGs | | | Refer to the FG specifications table in this document |
| Modulating signal source | | AWGs | | | Refer to the AWG specifications table in this document |
| **Amplitude and offset modulators (16-bit modulating waveform)** | | | | | |
| Deviation | -Dev. gain | | +Dev. gain | $V_p$ | |
| Modulating signal resolution | | 16 | | Bits | AWG waveform |
| Modulating signal BW | 0 | | 500 | MHz | AWG Nyquist limit |
| Deviation gain | 0 | | 1.5 | $V_p$ | |
| Deviation gain resolution | | 14 | | Bits | Limited by the output DAC |
| **Amplitude and offset modulators (32-bit modulating waveform)** | | | | | |
| Deviation | -Dev. gain | | +Dev. gain | $V_p$ | |
| Modulating signal resolution | | 16 | | Bits | AWG waveform is truncated |
| Modulating signal BW | 0 | | 100 | MHz | AWG Nyquist limit |
| Deviation gain | 0 | | 1.5 | $V_p$ | |
| Deviation gain resolution | | 14 | | Bits | Limited by the output DAC |

## IQ modulators specifications

| Parameter | M3202A-CH4 | | | Units | Comments |
|---|---|---|---|---|---|
| | Min | Typ | Max | | |
| **General specifications** | | | | | |
| IQ modulators | | 4 | | | 1 per output channel |
| Carrier signal source | | FGs | | | Refer to the FG specifications table in this document |
| Modulating signal source | | AWGs | | | Refer to the AWG specifications table in this document |
| Amplitude deviation | –1.5 | | 1.5 | $V_p$ | |
| Phase deviation | –180 | | 180 | Deg | |
| I modulating signal resolution | | 16 | | Bits | AWG waveform |
| I modulating signal BW | 0 | | 500 | MHz | AWG Nyquist limit |
| Q modulating signal resolution | | 16 | | Bits | AWG waveform |
| Q modulating signal BW | 0 | | 500 | MHz | AWG Nyquist limit |

## Clock system specifications

| Parameter | M3202A-CH4 | | | Units | Comments |
|---|---|---|---|---|---|
| | Min | Typ | Max | | |
| **General specifications** | | | | | |
| Clock frequency | | 1.0 | | GHz | |

## AC performance

| Parameter | M3202A-CH4 | | | Units | Comments |
|---|---|---|---|---|---|
| | Min | Typ | Max | | |
| **General characteristics** | | | | | |
| Analog output jitter | | < 2 | | ps | RMS (cycle-to-cycle) |
| AWG trigger to output jitter | | < 2 | | ps | RMS (cycle-to-cycle) for any trigger referenced to the chassis clock; independent of input trigger jitter if input jitter < 4 ns peak-to-peak |
| Trigger resolution | | 10 | | ns | |
| Channel-to-channel skew | | < 20 | | ps | Between ch 0 and ch 1, and ch 2 and ch 3 |
| | | < 50 | | ps | Between any channel |
| | | < 150 | | ps | Between modules, chassis dependent |
| Clock output jitter | | < 2 | | ps | RMS (cycle-to-cycle) |
| Clock accuracy and stability | | 100 | | ppm | PXIe, PXIe versions; chassis dependent |
| **AC characteristics** | | | | | |
| Spurious-free dynamic range (SFDR) | | | | | $P_{out}$ = 0 dBm, measured from DC to max frequency |
| • $f_{out}$ = 10 MHz | | 68 | | dBc | |
| • $f_{out}$ = 40 MHz | | 66 | | dBc | |
| • $f_{out}$ = 80 MHz | | 62 | | dBc | |
| • $f_{out}$ = 120 MHz | | 58 | | dBc | |
| • $f_{out}$ = 160 MHz | | 54 | | dBc | |
| • $f_{out}$ = 200 MHz | | 53 | | dBc | |
| • $f_{out}$ = 320 MHz | | 55 | | dBc | |
| • $f_{out}$ = 390 MHz | | 58 | | dBc | |
| Crosstalk (adjacent channels) | | | | | |
| • $f_{out}$ = 10 MHz | | < –105 | | dB | |
| • $f_{out}$ = 40 MHz | | –85 | | dB | |
| • $f_{out}$ = 80 MHz | | –80 | | dB | |
| • $f_{out}$ = 120 MHz | | –89 | | dB | |
| • $f_{out}$ = 160 MHz | | –76 | | dB | |
| • $f_{out}$ = 200 MHz | | –86 | | dB | |
| • $f_{out}$ = 320 MHz | | –83 | | dB | |

| Parameter | M3202A-CH4 | | | Units | Comments |
|---|---|---|---|---|---|
| | Min | Typ | Max | | |
| Crosstalk (non-adjacent channels) | | | | | |
| • $f_{out}$ = 10 MHz | | < –105 | | dB | |
| • $f_{out}$ = 40 MHz | | –89 | | dB | |
| • $f_{out}$ = 80 MHz | | –81 | | dB | |
| • $f_{out}$ = 120 MHz | | –103 | | dB | |
| • $f_{out}$ = 160 MHz | | –95 | | dB | |
| • $f_{out}$ = 200 MHz | | –102 | | dB | |
| • $f_{out}$ = 320 MHz | | –97 | | dB | |
| **AC characteristics** | | | | | |
| Phase noise (SSB) | | | | | |
| Offset = 1 kHz | | < –127 | | dBc/Hz | |
| Offset = 10 kHz | | < –133 | | dBc/Hz | |
| Offset = 100 kHz | | < –138 | | dBc/Hz | |
| Average noise power density | | < –145 | | dBm/Hz | |
| Phase noise (SSB) | | | | | |
| Offset = 1 kHz | | < –127 | | dBc/Hz | |

This value corresponds to a chassis that fulfils the PXI Express specifications. This value can be improved with an external chassis clock or a System Timing Module.

This value corresponds to an M9005A PXIe chassis.

## AC performance, typical

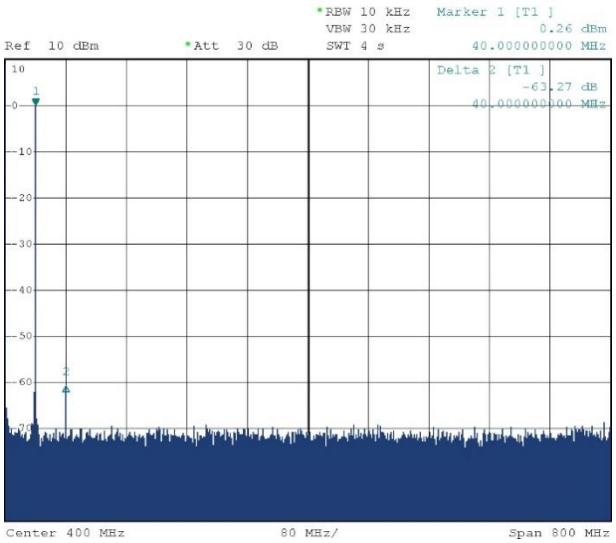


Figure 2. Single-tone spectrum @ $f_{out}$ = 40 MHz

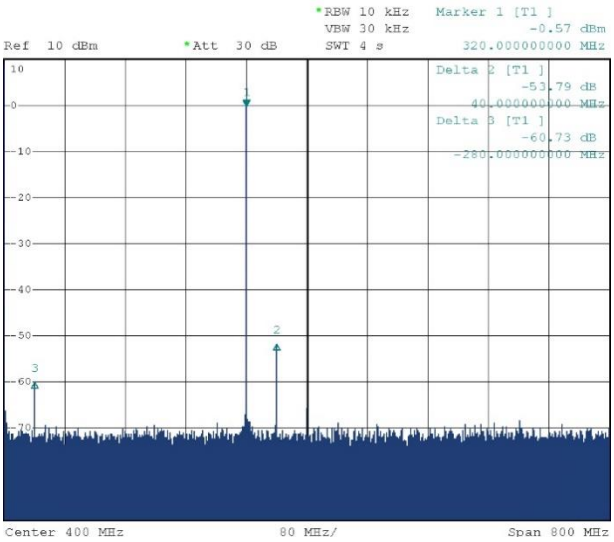


Figure 3. Single-tone spectrum @ $f_{out}$ = 160 MHz

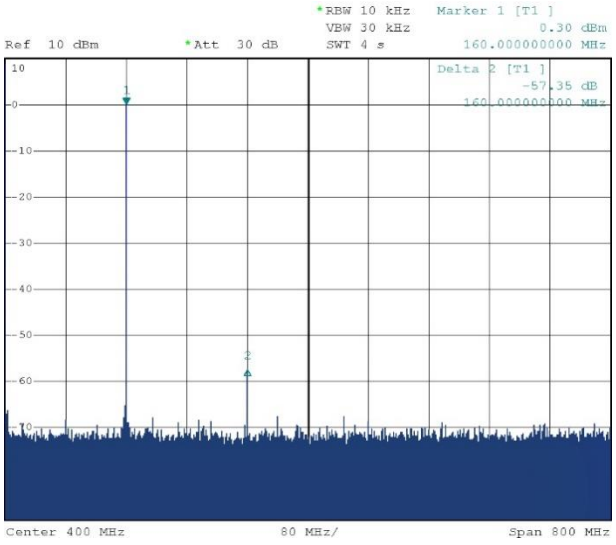


Figure 4. Single-tone spectrum @ $f_{out}$ = 320 MHz

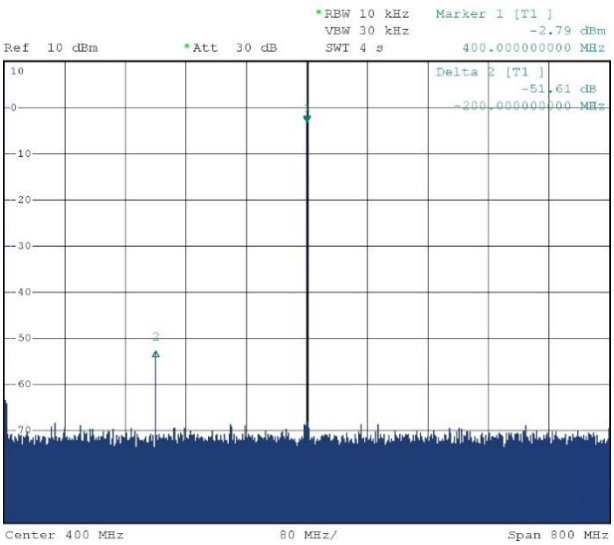


Figure 5. Single-tone spectrum @ $f_{out}$ = 400 MHz

# System Specifications

## Environmental specifications (PXI Express)

| Parameter | M3202A-CH4 | | | Units | Comments |
|---|---|---|---|---|---|
| | Min | Typ | Max | | |
| **System bus** | | | | | |
| Slots | | 1 | | Slot | PXI Express (CompactPCI Express compatible) |
| PCI Express type | Gen 1 | | Gen 2 | – | Automatic gen negotiation, chassis dependent |
| PCI Express link | 1 | | 4 | Lanes | Automatic lane negotiation, chassis dependent |
| PCI Express speed | 400 | | 1600 | MBytes/s | Depends on # of lanes, chassis, congestion |
| **Power and temperature** | | | | | |
| 3.3 V PXIe power supply | | 1.5 | | A | ~ 5 W |
| 12 V PXIe power supply | | 2 | | A | ~ 24 W |

| Environmental [1] | | |
|---|---|---|
| Temperature range | Operating | 0 to +45 °C (10,000 feet) |
| | Non-operating | -40 to +70 °C (up to 15,000 feet) |
| Max operative altitude | | 4000 m (10,000 feet) |
| Operating Humidity range (%RH) | | 10 to 95% at 40 °C |
| Non-operating Humidity range (%RH) | | 5 to 95% |
| Calibration interval | | 1 year |
| EMC | | Complies with European EMC Directive<br>• IEC/EN 61326-1<br>• CISPR Pub 11 Group 1, class A<br>This ISM device is in compliance with Canadian ICES-001.<br>Cet appareil ISM est conforme à la norme NMB-001 du Canada.<br>This ISM device is in compliance with Australian and New Zealand RCM.<br>This ISM device is in compliance with South Korea EMC KCC. |

1. Samples of this product have been type tested in accordance with the Keysight Environmental Test Manual and verified to be robust against the environmental stresses of Storage, Transportation and End-use; those stresses include but are not limited to temperature, humidity, shock, vibration, altitude and power line conditions. Test Methods are aligned with IEC 60068-2 and levels are similar to MIL-PRF-28800F Class 3.

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